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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/642,519	08/18/2003	Naoki Kuwata	122.1561	1583
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STAAS & HALSEY LLP SUITE 700 1201 NEW YORK AVENUE, N.W. WASHINGTON, DC 20005			EXAMINER JOSEPH, JAISON	
			ART UNIT 2611	PAPER NUMBER
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No. 10/642,519	Applicant(s) KUWATA ET AL.	
	Examiner Jaison Joseph	Art Unit 2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 22 August 2007.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-8 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-5 is/are rejected.
- 7) ☒ Claim(s) 6-8 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Response to Arguments

Applicant's arguments filed 08/22/2007 have been fully considered but they are not persuasive.

Regarding claims 1-3, applicant argue, "[a]t page 4 of the Action ... Accordingly, claims 1 – 3 patentably distinguish over soda". However Examiner respectfully disagrees. Applicant Admitted Prior Art (AAPA) discloses a timing extraction circuit which uses a PLL circuit containing a phase comparator circuit for performing a phase comparison between a data signal of bit rate B and a clock signal of $B/2$ at intervals of $2/B$ (see figure 3), AAPA does not expressly disclose the timing extraction circuit further comprise a detection circuit for detecting the absence of an output of phase comparison information (i.e. collapse of synchronization, AAPA discloses "during that period (receiving a prescribed pattern) ... the PLL running out of synchronization" (page 8, 12 – 14)) from said phase comparator circuit by receiving a data signal of prescribed pattern; and a control circuit for controlling the phase of said clock signal in order to maintain synchronization. In analogous art, Soda et al teach detector circuit in PLL circuitry to detect the output of the phase comparator indicates a collapse of synchronization and controlling the oscillation of a VCO to maintain in synchronization (see figure 2, component 23 and column 4, line 14 – 33) [Applicant admits that when the PLL circuit receives a prescribed pattern, the PLL will run out of synchronization (i.e. if the prescribed pattern is detected (absence of the comparison output), it will indicate the possible collapse of the synchronization). Soda teaches a detector detecting the

collapse of the synchronization from the output of the phase comparator is equivalent to detecting the prescribed pattern (absence of the comparison output).]. Therefore, AAPA in view of Soda teach all cited limitations. Thus Examiner maintains the rejection of claims 1 – 3. Furthermore, Applicant is reminded that the examiner is entitled to give broadest reasonable interpretation to the language of the claims.

Regarding claim 4, Applicant argue, "In operation of the circuit ... solves the above problems caused by the circuit of AAPA" However Examiner respectfully disagrees. AAPA discloses a timing extraction circuit which uses a PLL circuit containing a phase comparator circuit for performing a phase comparison between a data signal of bit rate B and a clock signal of $B/2$ at intervals of $2/B$ (see figure 3 components 45, 46 page 4, line 11 – page 5, line 4 of the present specification) AAPA further discloses said phase comparator circuit comprises two phase comparator circuits which respectively accepts phases differing by one cycle of said data signal to perform comparisons for all data signals (see figure 3, components 45, 46 and page 4, line 11 – page 5, line 4 of the present specification) as recited in claim 4. Thus AAPA teaches all cited limitations. Therefore Examiner maintains the rejection of claim 4.

Regarding claim 5, Applicant argues, "[i]n the rejection of claim 5 ... patentably distinguish over the references and rejection of record." However examiner respectfully disagrees. Blum teaches, as applicant admitted, a circuit for detecting a duty cycle of a clock signal and after the detection generate a control signal (correcting the duty cycle) (see page 8 of the remarks). Further Blum clearly teach in figure 1 a duty cycle evaluation circuit for evaluating a duty cycle between input data before and after a point

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at which said PLL circuit is locked (see figure 1); and a control circuit for controlling, based on a result of said evaluation, a data discrimination phase (adjusting the duty cycle) before and after the point at which said PLL circuit is locked (see figure 1). Thus AAPA in view of Blum teach all cited limitations. Therefore Examiner maintains the rejection of claim 5.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

Claim 4 is rejected under 35 U.S.C. 102(a) as being anticipated by Applicant Admitted Prior Art (AAPA).

Regarding claim 4, AAPA discloses a timing extraction circuit which uses a PLL circuit containing a phase comparator circuit for performing a phase comparison between a data signal of bit rate B and a clock signal of B/2 at intervals of 2/B (see figure 3 components 45, 46 page 4, line 11 – page 5, line 4 of the present specification) AAPA further discloses said phase comparator circuit comprises two phase comparator circuits which respectively accept phases differing by one cycle of said data signal to perform comparisons for all data signals (see figure 3, components 45, 46 and page 4, line 11 – page 5, line 4 of the present specification).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1 – 3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant Admitted Prior Art (AAPA) in view of Soda (US Patent 5,956,378).

Regarding claim 1, AAPA discloses a timing extraction circuit which uses a PLL circuit containing a phase comparator circuit for performing a phase comparison between a data signal of bit rate B and a clock signal of $B/2$ at intervals of $2/B$ (see figure 3), AAPA does not disclose the timing extraction circuit further comprise a detection circuit for detecting the absence of an output of phase comparison information from said phase comparator circuit by receiving a data signal of prescribed pattern; and a control circuit for controlling upon detecting said absence, the phase of said clock signal in order to maintain synchronization.

In analogous art, Soda teaches a PLL circuit comprising a detection circuit for detecting the absence of an output of phase comparison information from said phase comparator circuit by receiving a data signal of prescribed pattern; and a control circuit for controlling upon detecting said absence, the phase of said clock signal in order to maintain synchronization (see figure 2, component 23 and column 4, line 14 – 33).

Therefore it would be obvious to an ordinary skilled in the art at the time the invention was made to incorporate the Soda's PLL control circuit in AAPA to have a phase locking

loop circuit which need not have an adjusting terminal for use in adjusting the frequency range.

Regarding claim 2, which inherits the limitations of claim 1, Soda further teaches control circuit controls the phase of said clock signal by inverting said clock signal (see column 6, lines 15 –39).

Regarding claim 3, which inherits the limitation of claim 1, Soda further teaches said control circuit controls the phase of said clock signal by controlling a VCO.

Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant Admitted Prior Art (AAPA) in view of Blum (US Patent 5,757,218).

Regarding claim 5, AAPA discloses a timing extraction circuit which uses a PLL circuit containing a phase comparator circuit for performing a phase comparison between a data signal of bit rate B and a clock signal of $B/2$ at intervals of $2/B$ (see figure 3), AAPA does not disclose a duty cycle evaluation circuit and a control circuit controlling the signal in response to the duty cycle evaluation circuit. However in analogous art, Blum teaches a duty cycle evaluation circuit for evaluating a duty cycle between input data before and after a point which said PLL circuit is locked (see figure 1, component 14), and a control circuit for controlling, based on a result of said evaluation, a data discrimination phase before and after the point at which said PLL circuit is locked (see figure 1, component 106). Therefore it would be obvious to an ordinary skilled in the art at the time the invention was made to incorporate Blum's duty cycle correction circuit in AAPA to correct the duty cycle and compensates for error introduced by intervening circuits.

Allowable Subject Matter

Claims 6 – 8 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jaison Joseph whose telephone number is (571) 272-6041. The examiner can normally be reached on M-F 9:30 - 6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chieh Fan can be reached on (571) 272-3042. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Jaison Joseph
11/08/2007


CHIEH M. FAN
SUPERVISORY PATENT EXAMINER